REMARKS

Claims 1, 3-4, 6-12 and 14-30 are pending in this application. For purposes of expedition, claims 2, 5 and 13 have been canceled without prejudice or disclaimer. Independent claims 1 and 9 have been amended to incorporate all the limitations of the allowed dependent claims 5 and 13 in order to place the instant application in condition for allowance. Claims 3-4, 6-7, and 14 have been amended to ensure proper dependency among the claims as pending, in view of the cancellation of claims 2, 5 and 13 and the amendment of claims 1 and 9, in accordance with current Office policy, to alternatively define the disclosed invention over the prior art of record and expedite compact prosecution of the instant application. Accordingly, entry of the foregoing amendments is proper under 37 C.F.R. §1.116(b) because those amendments simply respond to the issues raised in the final rejection, no new issues are raised, no further search is required, and the foregoing amendments are believed to remove the basis of the outstanding rejections and to place all claims in condition for allowance. The foregoing amendments, or explanations, could not have been made earlier because these issues had not previously been raised.

Claims 5-7, 13-14, 19-20, 24-25 and 29-30 have been conditionally allowed if rewritten in independent form to include all of the limitations of their respective base claims 1, 9, 16, 21 and 26. The Examiner's indication of allowability of these claims is noted with appreciation. As previously discussed, and in the interest of expedition, the subject matter of the allowed claim 5 and 13 have been incorporated into their

respective base claims 1 and 9 in order to place claims 1, 3-4, 6-8 and claims 9-12 and 14-15 in condition for allowance. As for claims 19-20, 24-25 and 29-30, forbearance is respectfully requested pending Applicants' traversal of the outstanding rejection of parent claims 16, 21 and 26.

Claims 16-17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Horstmann et al., U.S. Patent No. 6,125,433, as modified to incorporate selected features from Watkins, U.S. Patent No. 5,937,436. In support of this rejection, the Examiner alleges that Horstman '433, as a primary reference, teaches an apparatus which stores translation and protection table (TPT) entries for virtual to physical address translations (e.g., col. 4, lines 54-60), and which flushes individual translation and protection table (TPT) entry stored in accordance with a corresponding translation cacheable flag (i.e., valid bit) (e.g., col. 4, lines 30-34, col. 11, lines 25-35) included in the individual translation table entry (e.g., fig. 6, VB+0; col. 7, lines 6-8; col. 11, lines 34-36).

Again, the Examiner has expressly admitted that Horstmann '433 does **not** disclose the use of protection in the translation table entries. However, the Examiner alleges that the use of protection in the translation table entries are described on col. 4, lines 41-45; col. 7, lines 55-64 of Watkins '436 which would enable one skilled in the art to make the modification in order to arrive at Applicants' claims 16-17.

This rejection is respectfully traversed, however. Applicants respectfully submit that features of the present invention are not taught or suggested by Horstmann '433 and Watkins '436, whether taken individually or in combination with any other references of record. Therefore, Applicants respectfully traverse the rejection and

request the Examiner to reconsider and withdraw this rejection for the following reasons.

Independent claim 16 requires an apparatus comprising a storage device which stores translation and protection table (TPT) entries for virtual to physical address translations, and a mechanism which flushes individual translation and protection table (TPT) entry stored in the storage device in accordance with a corresponding translation cacheable flag included in the individual translation and protection table (TPT) entry.

In other words, each TPT entry stored in the storage device has a corresponding translation cacheable flag used to enable the mechanism to flush individual TPT entry in accordance with the translation cacheable flag.

In contrast to Applicants' independent claim 16, Horstmann '433 discloses the use of a cache dedicated to virtual address translations, called a translation lookaside buffer (TLB) and memory management software (MMU) used to allocate main memory to a process and store physical page number for each virtual page in the TLB in the main memory.

As shown in FIG. 5, the translation buffer (TLB) of Horstmann '433 includes a content addressable memory (CAM) column 10, a least recently used (LRU) column 11, and a random access memory (RAM) column 12. The LRU column 11 contains 64 ripple counters used to control the replacement of translation entries stored in the CAM and RAM columns.

Each row formed by the adjacent CAM, RAM and LRU columns is referred as a slice. Each slice includes a virtual page number storage location in CAM column 10, a corresponding physical page number storage location in RAM column 12, and an

associated value within the LRU counter of that slice. When the MMU (memory management unit) receives a virtual page number, the "valid bits" are provided from the MMU to the translation buffer (TLB) and compared to the virtual page number entries stored within each of the 64 locations in the CAM column 10. These associated bits are **not** part of the slice or row of the adjacent CAM, RAM and LRU columns shown in FIG. 5. Rather, these bits are provided by the MMU to indicate whether the corresponding slices contain valid virtual to physical translation entries. At initial operations of the translation buffer (TLB), each valid bit is reset which indicates that none of the slices contain valid translation entries. When a translation entry is loaded into a slice, the valid bit included in the slice is set using the LRU algorithm to indicate that the slice contains a valid translation entry, see column 7, lines 5-30 of Horstmann '433. Therefore, the function of the valid bit as described by Horstmann '433 is to indicate whether a slice in the translation table (TLB) contains a valid translation entry. However, these bits are **not** part of the TLP entries.

In other words, there is **no** disclosure anywhere from Horstmann '433 of Applicants' use of a corresponding translation cacheable flag within an individual translation and protection table (TPT) entry in order to flush the individual TPT entry in accordance with the corresponding translation cacheable flag included in the TPT entry as expressly defined in claims 16-17.

Nevertheless, the Examiner cites FIG. 6, column 7, lines 6-8, and column 11, lines 34-36 of Horstmann '433 for allegedly disclosing the use of a corresponding

translation cacheable flag (i.e., valid bit) included in the individual translation table entry for flushing purposes.

However, this citation is misplaced. FIG. 6 of Horstman '433 only shows a slice or row of the adjacent CAM, RAM and LRU columns shown in FIG. 5. The cited column 7, lines 6-8 of Horstman '433 simply confirms that the slice or row of the adjacent CAM, RAM and LRU columns.

Likewise, the cited column 11, lines 34-36 of Horstman '433 refers to the use of a level decoding circuit 15 of each slice to determine whether a match or bit occurs for one of the slices. If a hit occurs, the valid bit [associated with the slice] is reset.

As previously discussed, the valid bit of Horstmann '433 is **not** included in each translation entry and is **not** used for the purpose of flushing a corresponding translation entry as alleged by the Examiner. In Horstmann '433, the flushing is performed by comparing the entry virtual page address with each translation entry within the TLB, and only when there is a match, resetting the valid bit to indicate that the slice is ready to receive another valid translation entry.

As a secondary reference, Watkins '436 does **not** remedy the deficiency of Horstmann '433. As correctly relied upon by the Examiner, Watkins '436 simply describes the use of protection bits 285 in a sample physical translation format 281 as shown in FIG. 2B in determining if a page is accessible using the physical translation for the virtual address as described on column 4, lines 41-45 and column 7, lines 55-64. However, Watkins '436 does **not** suggest the use of a translation cacheable flag

included in each TPT entry for determining whether to flush the individual TPT entry as defined in claims 16-17.

The law under 35 U.S.C. §103 is well settled that "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." ACS Hospital System, Inc v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). The Examiner must point to something in the prior art that suggests in some way a modification of a particular reference or a combination of references in order to arrive at Applicants' claimed invention. Absent such a showing, the Examiner has improperly used Applicants' disclosure as an instruction book on how to reconstruct to the prior art to arrive at Applicants' claimed invention.

In order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and **not** based on Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143. In other words, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981,

180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USQP 494, 496 (CCPA 1970).

In the present situation, the Examiner has incorrectly interpreted the teachings of Horstmann '433, failed to consider all the key limitations of Applicants' claims 16-17, and failed to provide any suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify Watkins '436 into Horstmann '433 in order to arrive at Applicants' claims 16-17. Therefore, Applicants respectfully request that the rejection of claims 16-17 be withdrawn.

Dependent claim 18 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Horstmann et al., U.S. Patent No. 6,125,433, as modified to incorporate selected features from Watkins, U.S. Patent No. 5,937,436 and Futral, U.S. Patent No. 6,112,263. In support of this rejection, the Examiner further cites Futral >263 for disclosing the use of a host comprising a host memory on column 1, lines 37-45; column 7, lines 47-55; and FIGs. 2A which enables one skilled in the art to make the appropriate modification in order to arrive at Applicants' claim 18. Applicants respectfully traverse this rejection for reasons discussed against the rejection of claims 16-17, that is, Horstmann '433 only describes the use of a valid bit to indicate if a slice contains a valid entry, and does not describe the use of a translation cacheable flag included in each TPT entry for flushing purposes.

Claims 1-4, 8-12, 15, 21-23 and 26-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Watkins, U.S. Patent No. 5,937,436, as modified to

incorporate selected features from Horstmann et al., U.S. Patent No. 6,125,433, and Futral, U.S. Patent No. 6,112,263. In support of this rejection, the Examiner argues mostly that Watkins '436 does **not** describe the use of flushing a translation entry in accordance with a translation cacheable flag. The Examiner also cites Horstmann '433 for disclosing this feature and Futral '263 for disclosing the use of a host including a host memory to enable one skilled in the art to make the appropriate modification to arrive at Applicants' claims 1-4, 8-12, 15, 21-23 and 26-28. For purposes of expedition, independent claims 1 and 9 have been amended to incorporate all the limitations of the allowed claims 5 and 13. As a result, claims 1, 3-4, 6-8, 9-12 and 15 are believed to be in condition for allowance.

To the extent that the rejection may still be applicable for claims 21-23 and 26-28, Applicants respectfully traverse the rejection for reasons discussed against the rejection of claims 16-17 that is, Horstmann '433 only describes the use of a valid bit provided by the MMU that is associated with a slice in the translation buffer (TLB) in order to indicate if a slice contains a valid entry, and does **not** describe the use of a translation cacheable flag included in each TPT entry for flushing purposes.

In contrast to Watkins '436, Horstmann '433, and Futral '263, Applicants' independent process claim 21 requires:

> storing, in a cache of an adapter installed in a host system and provided to interface a switched fabric, translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag; and

> checking a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache of the adapter to determine whether to discard one or more selected TPT entries from the cache of the adapter.

Likewise, Applicants' independent system claim 26 defines an adapter in a host system provided to interface a switch fabric comprising:

> a cache to store translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag; and
>
> a mechanism to determine a status of the translation cacheable flag of one or more selected TPT entries stored in the cache, and to discard the one or more selected TPT entries from the cache based on the status of the translation cacheable flag.

Again, there is **no** disclosure anywhere from the Examiner's proposed combination, including Watkins '436, Horstmann '433, and Futral '263, of Applicants' use of a translation cacheable flag included in each TPT for discarding the TPT entry based on the status of the translation cacheable flag.

Again, in view of the Examiner's incorrect assessment of Watkins '436, Horstmann '433, and Futral '263, and the failure to address the key limitations of Applicants' use of a translation cacheable flag included in each TPT for discarding the TPT entry based on the status of the translation cacheable flag, Applicants respectfully request that the rejection of claims 21-23 and 26-28 be withdrawn.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed

to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

INTERVIEW:

In the interest of expediting prosecution of the present application, Applicants respectfully request that an Examiner interview be scheduled and conducted. In accordance with such interview request, Applicants respectfully request that the Examiner, after review of the present Amendment, contact the undersigned local Washington, D.C. area attorney at the local Washington, D.C. telephone number (703) 312-6600 for scheduling an Examiner interview, or alternatively, refrain from issuing a further action in the above-identified application as the undersigned attorneys will be telephoning the Examiner shortly after the filing date of this Amendment in order to schedule an Examiner interview. Applicants thank the Examiner in advance for such considerations. In the event that this Amendment, in and of itself, is sufficient to place the application in condition for allowance, no Examiner interview may be necessary.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 of

Antonelli, Terry, Stout & Kraus, LLP (referencing Attorney Docket No. 219.37373X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 2, 5, and 13 have been canceled without prejudice or disclaimer. **Claims 1, 3-4, 6-7, 9 and 14** have been amended, as follows:

1. (Amended) A host coupled to a switched fabric including one or more fabric-attached I/O controllers, comprising:

a processor;

a host memory coupled to said processor; and

a host-fabric adapter coupled to said processor and provided to interface with said switched fabric, ~~which~~including an internal cache to store ~~caches~~ selected translation and protection table (TPT) entries from said host memory for a data transaction, each TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory, a translation cacheable flag to specify whether said host-fabric adapter may flush a corresponding TPT entry, a physical page address field to address a physical page frame of data entry, and a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory;

~~and flushes~~wherein said host-fabric adapter is configured to flush individual cached translation and protection table (TPT) entry from said internal cache in

accordance with ~~a~~the corresponding translation cacheable flag.

3. (Amended) The host as claimed in claim ~~2~~1, wherein each of said selected translation and protection table (TPT) entries represents translation of a single page of said host memory.

4. (Amended) The host as claimed in claim ~~2~~1, wherein said host-fabric adapter is provided to perform virtual to physical address translations and validate access to said host memory using said selected translation and protection table (TPT) entries.

6. (Amended) The host as claimed in claim ~~5~~1, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether said host-fabric adapter can write to page; a RDMA Read Enable flag which indicates whether the page can be source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be target of RDMA Write operation.

7. (Amended) The host as claimed in claim ~~5~~1, wherein said host-fabric adapter flushes a designated cached translation and protection table (TPT) entry from said internal cache when said translation cacheable flag of said designated cached translation and protection table (TPT) entry indicates a first logic state, and maintains

said designated cached translation and protection table (TPT) entry in said internal cache when said translation cacheable flag of said designated cached translation and protection table (TPT) entry indicates a second logic state opposite of said first logic state.

9. (Amended) A network, comprising:

a switched fabric;

I/O controllers attached to said switched fabric; and

a host comprising an operating system, a host memory, and a host-fabric adapter ~~which caches selected~~including translation and protection table (TPT) entries ~~from said host memory~~, each TPT entry comprising protection attributes to control read and write access to a given memory region of the host memory, a translation cacheable flag to specify whether the host-fabric adapter may flush a corresponding TPT entry, a physical page address field to address a physical page frame of data entry, and a memory protection tag to specify whether the host-fabric adapter has permission to access the host memory, ~~and which flushes~~

wherein the host-fabric adapter is configured to cache selected TPT entries from the host memory and to flush individual cached translation and protection table (TPT) entry in accordance with ~~a~~the corresponding translation cacheable flag.

14. (Amended) The network as claimed in claim ~~13~~9, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether said host-fabric adapter can write to page; a RDMA Read Enable flag which indicates whether the page can be source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be target of RDMA Write operation.